FPA-320x256-Dip InGaAs Array

Version V1.00

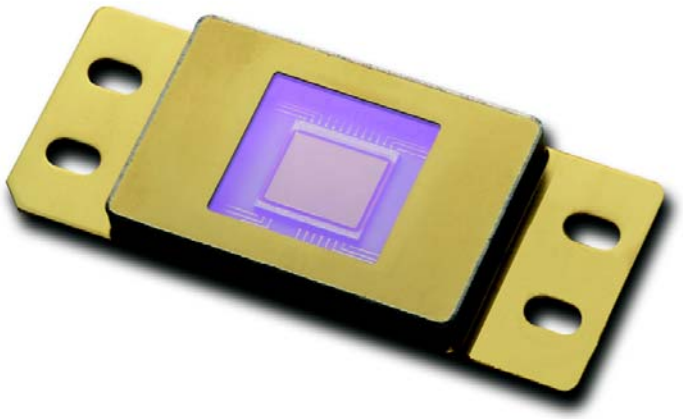
NEAR INFRARED (0.9um-1.7um) IMAGE SENSOR

FEATURES

- Room Temperature Operation
- 320x256 Array Format
- 28-pin Metal DIP Package
- Embedded Thermoelectric Cooler
- Typical Pixel Operability >99.5%
- Quantum Efficiency >70%

APPLICATIONS

- Near-infrared Imaging
- Imaging Spectroscopy
- Covert Surveillance
- Semiconductor Inspection
- Medical Science and Biology
- Fiberoptic Telecommunication
- Astronomy and Scientific
- Industrial Thermal Imaging
- Moisture Mapping



GENERAL DESCRIPTIONS

PARAMETER	VALUE
Sensor Technology	Standard InGaAs/InP
Spectral Range	0.9um-1.7um
Image Format	320(H)x256(V)
Pixel Pitch	30umx30um (>99% Fill Factor)
Image Size	9.6mm(H)x7.68mm(V)
Package Type	28-pin Metal DIP Package
Weight	24.6g

FPA CHARACTERISTICS (T_a=25°C)

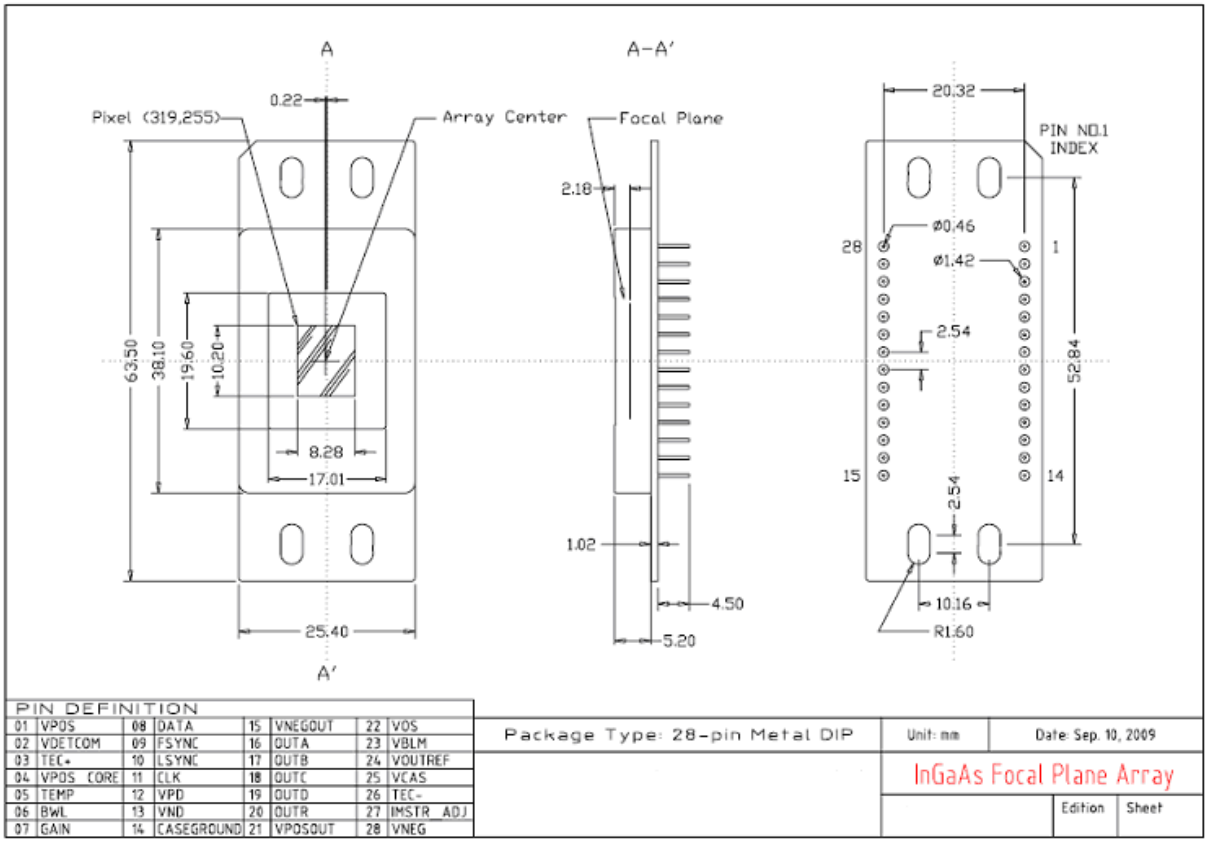
PARAMETER	TYPICAL	CONDITIONS
Dark Current	≤ 0.4 pA	Pixel bias =0.1 volt
Quantum Efficiency	≥ 70%	λ=1.0um-1.6um
Fill Factor	>99%	
Adjacent pixel crosstalk	<1%	
Detectivity	≥ 5x10^{11} Jones	T_{int}=16ms, High Gain, λ=1.55um
Response Nonuniformity	≤ 10%	Under 50% Saturation
Nonlinearity (Max. Deviation)	≤ 2%	Over 10%-90% Full Well Capacity
Max. Pixel Rate	10MHz	
Gain	High: 13.3 uV/e$^-$ Low: 0.7 uV/e$^-$	
Pixel Operability*	> 99.5%	Dark Current ≤20% Full Well Response Nonuniformity ≤ 20%

* Pixel Operability is defined within the center 318x254 region

ABSOLUTE MAXIMUM RATINGS

PARAMETER	UNIT	MIN	MAX
Operation Temperature	°C	-20	85
Storage Temperature	°C	-40	85
Power Consumption	mW	---	175

PACKAGE OUTLINE



Note : ID number of the imager is printed on the flank of the package

OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
12	VPD	5.5V	<1mA	Logic positive supply
13	VND	0V	<1mA	Logic negative supply
21	VPOSOUT	5.5V	<25mA	Output stage analog supply
15	VNEGOUT	0V	<25mA	Output stage analog ground
1	VPOS	5.5V	<5mA	Positive analog supply
28	VNEG	0V	<15mA	Negative analog supply and substrate
4	VPOS_CORE	5.5V	<15mA	CTIA amplifier positive supply
2	VDETCOM	4.7V - 5.5V	<5mA	Detector common voltage Detector bias = VDETCOM-4.7*

*VDETCOM lower than 4.7V will forward bias the sensor

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
11	CLK	0V - 5.5V	<10ns	Master clock Max. Freq.=5MHz
9	FSYNC	0V - 5.5V	<10ns	Frame sync - controls frame start and integration time
10	LSYNC	0V - 5.5V	<10ns	Line sync - controls line readout timing
8	DATA	0V - 5.5V	<10ns	Data code input - programs device function registers in Control Mode Left open in Default Mode

Clocks	Synchronization
FSYNC	Rising and falling when CLK is rising
LSYNC	Rising and falling when CLK is falling
DATA	Rising (falling) when CLK is rising (falling)

Video Output

Pin #	Outputs	Levels	Settle	Remark
16	OUTA	1.4V to 4.1V	<50ns to 0.1%	Output A used in single output mode
17	OUTB	1.4V to 4.1V	<50ns to 0.1%	Output A and B used in two output mode
18	OUTC	1.4V to 4.1V	<50ns to 0.1%	Output A, B, C, and D used in four output mode
19	OUTD	1.4V to 4.1V	<50ns to 0.1%	Output A, B, C, and D used in four output mode
20	OUTR	3V	-	Reference for common mode output

Gain & Bandwidth Selection in Default Mode

Pin #	Functions	Low	High	Remark
7	GAIN	0V C=10fF	5.5V C=210fF	Selects unit cell integration capacitor Left open in Control Mode
6	BWL	0V Low BW	5.5V High BW	Selects bandwidth limiting capacitor in unit cell Left open in Control Mode

Advanced Function

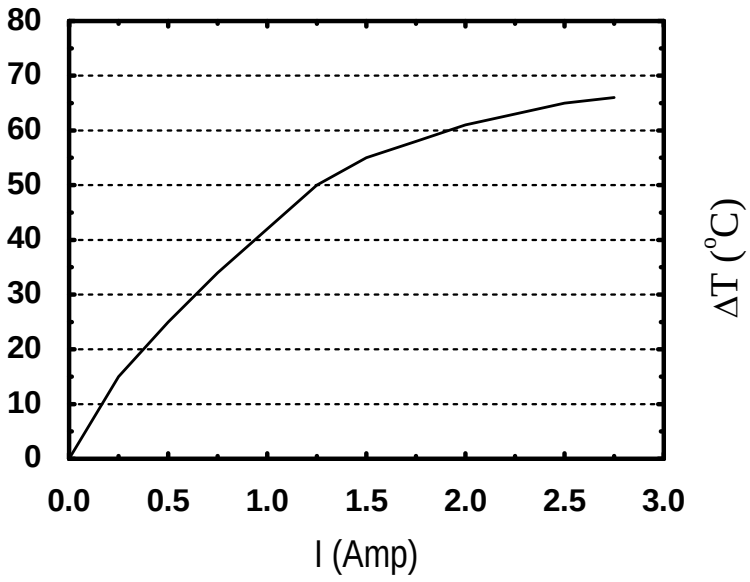
Pin #	Functions	Voltages	Remark
25	VCAS*	3.75V	CTIA amplifier cascode FET bias
24	VOUTREF*	3V	Output reference level during blanking period
23	VBLM*	2V	Detector bloom control
27	IMSTR_ADJ**	0V - 5.5V	Adjusts analog master bias current
22	VOS	0V - 5.5V	Variable Offset/Skimming Control Voltage
5	TEMP	0V - 5.5V	On chip temperature monitor 0.74V at 300K, **Slope=-14.8mV/10K in 50-300K**
14	CASE GROUNG	-	Kovar metal package shielding connection

*Internally generated after bias input, but can be overridden.
** Also addressable through control register (DATA).

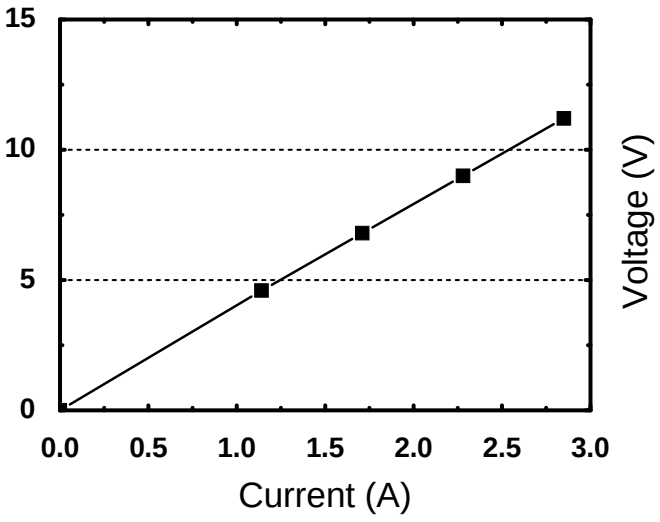
THERMOELECTRIC COOLER DATA

$\triangle T_{max}$	I_{max}	V_{max}
66℃	2.85A	11.3V

TEC Temperature Difference versus Current

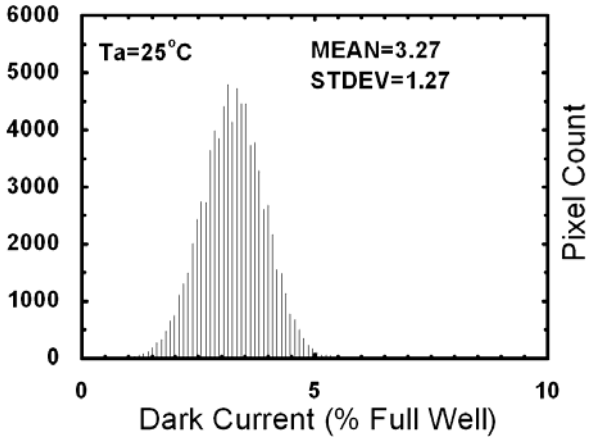


TEC Voltage versus Current

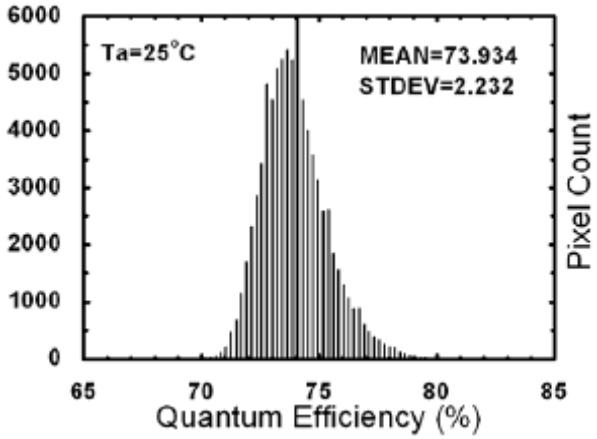


EXAMPLE CURVES

Statistical Histogram of Dark Current

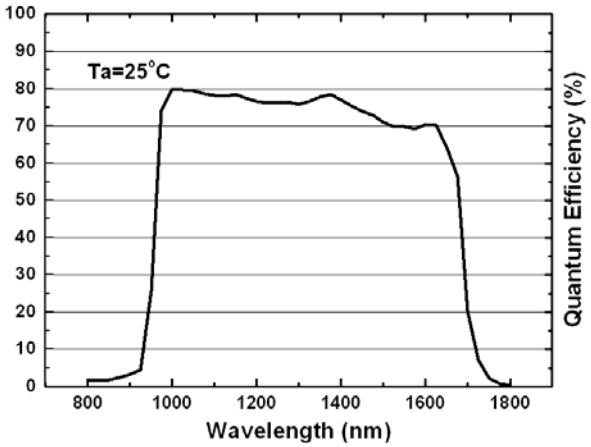


Test Conditions:	
Illumination	Dark
Wavelength	---
Gain	Low
Integration Time	16ms
Remark	Effective Screen



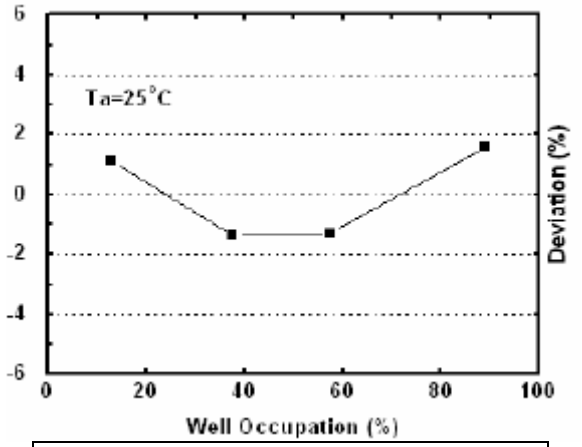
Test Conditions:	
Illumination	Nonuniformity≤± 0.15%
Wavelength	1310nm
Gain	Low
Integration Time	For 50% Saturation
Remark	Effective Screen

Quantum Efficiency Spectrum



Test Conditions:	
Illumination	Nonuniformity≤± 0.15%
Wavelength	Broadband
Gain	Low
Integration Time	2ms
Remark	Effective Screen Array Average

Linearity



Test Conditions:	
Illumination	Nonuniformity≤± 0.15%
Wavelength	1310nm
Gain	Low
Integration Time	---
Remark	Effective Screen Array Average

Statistical Histogram of Quantum Efficiency

TIMING CHART FOR DEFAULT MODE OPERATION